APLUS MAKE YOUR PRODUCTION A-PLUS

VOICE OTP IC

*a*P89682K – 682sec

*a*P89341K – 341sec

*a*P89170K – 170sec

*a*P89085K – 85sec

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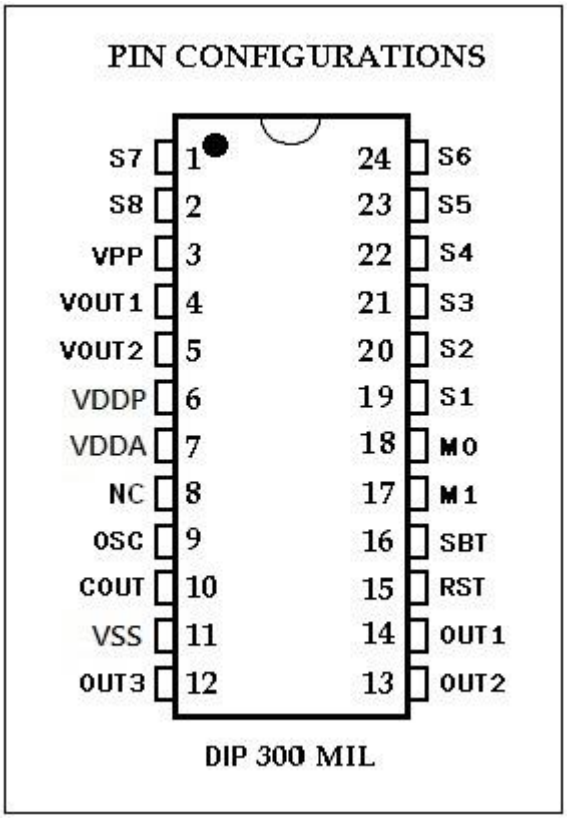
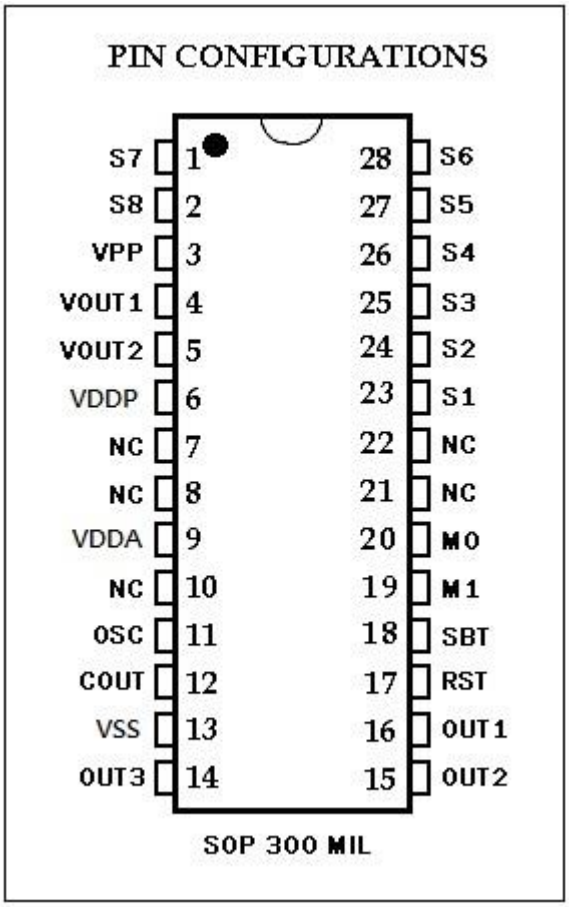
▪ FEATURES :

- Standard CMOS process.
- Embedded 16M/8M/4M/2M EPROM.
- **682/341/170/85** sec Voice Length at 6KHz sampling and 4-bit ADPCM compression.
- Maximum 1024 voice groups.
- Maximum 48KHz sample rate.
- Combination of voice blocks to extend playback duration.
- User selectable PCM16 or ULAW5 or PCM8 or ADPCM4 data compression
- 6 triggering modes are available :
  - Key Mode :
    S1 ~ S8 to trigger up to 57 voice groups;
    SBT to trigger up to 1024 voice groups sequentially;
    Power on play function.
  - CPU Parallel Mode :
    S[8:1] services as 8-bits address to trigger up to 256 voice groups
    with SBT goes HIGH to strobe the address bits.
  - SPI Mode : CS , SCK , DI
    3 wire address control up to 1024 voice groups.
  - I2C Mode : SCK , DI
    2 wire address control up to 1024 voice groups.
  - MP3 Mode :
    S1:Backward , S2: Forward , S3:Stop , S4:Reset ,
    SBT: Play/Pause Trigger up to 1024 voice groups.
  - aP89 Mode – Function setting compatible aP89341/aP89170/aP89085
- Voice Group Trigger Options: Edge / Level; Hold / Unholdable; Retrigger / Non-retrigger.
- Optional 16ms or 65us selectable debounce time
- RST pin set HIGH to stop the playback at once
- LVR (Low voltage reset)
- programmable outputs pin out1,out2,out3 :
  for busy-H , busy-L , stop-H , stop-L , prog busy-H , prog busy-L , Loadbit
  LED flash (LED high active) , ~LED flash (LED low active)
- Three kind oscillator: Internal-Rosc、External-Rosc、Crystal.
- 2V – 5V single power supply and < 5uA low stand-by current.
- 16/8/4 level volume control setting available.
- Audio out 16 bit.
- PWM Vout1 and Vout2 drive speaker directly
- D/A COUT pin drives speaker through an external BJT
- Development System support voice compilation.

▪ DESCRIPTION :

aP89682K/341K/170K/085K series high performance Voice OTP is fabricated with Standard CMOS process with embedded 16M/8M/4M/2M bits EPROM. It can store up to 682/341/170/85 sec voice message with 4-bit ADPCM compression at 6KHz sampling rate. 16-bit PCM and 8-bit PCM is also available for user selecting. User selectable triggering and output signal options provide maximum flexibility to various applications. Built-in resistor controlled oscillator, 16-bit current mode DAC output and 14-bit current mode PWM direct speaker driving output minimize the number of external components. PC controlled programmer and developing software are available.





▪ PIN NAMES :

PIN (24-pin)	Playback Mode	OTP Program Mode	Description
1	S7		Trigger pin (I/O pin with internal pull-down)
2	S8		Trigger pin (I/O pin with internal pull-down)
3	VPP	VPP	Supply ground
4	VOUT1		PWM output to drive speaker directly
5	VOUT2		PWM output to drive speaker directly
6	VDDP	VDDP	Supply voltage
7	VDDA	VDDA	Analog supply voltage
8	NC		
9	OSC		Oscillator input
10	COUT		DAC current output
11	VSS	VSS	Supply ground
12	OUT3		Programmable output (I/O pin)
13	OUT2		Programmable output (I/O pin)
14	OUT1		Programmable output (I/O pin)
15	RST	RST	Reset pin (input pin with internal pull-down)
16	SBT		Trigger pin (I/O pin with internal pull-down)
17	M1		Mode select pin 1 (input with internal pull-down)
18	M0		Mode select pin 0 (input with internal pull-down)
19 ~ 24	S1~S6	S2、S3	Trigger pin (I/O pin with internal pull-down)

▪ PIN DESCRIPTIONS :

• S1 ~ S8 :

Input Trigger Pins:

- In Key Mode: S1 to S8 is used to trigger 57 Voice groups.
- In CPU Parallel Mode : this pin low to high [Latch] the address at S1(lsb) to S8(msb) and starts the voice playback.
- In SPI Mode :
  S1 is Chip Select (SC) pin to initiate the command input.
  S2 is the Serial Clock (SCK) pin which clocks the input command and data bits into the chip.
  S3 is the Data In (DI) pin in which command and data bits are shifted input into the chip.
- In I2C Mode :
  S2 is the Serial Clock (SCK) pin which clocks the input command and data bits into the chip.
  S3 is the Data In (DI) pin in which command and data bits are shifted input into the chip.
- In MP3 Mode :
  S1:Backward. S2 :Forward. S3:Stop. S4: Reset.
- In aP89 Mode : compatible with APLUS 1st Generation OTP IC (aP89341/aP89170/aP89085) usage.

- **SBT :**

Input Trigger Pin:
- In Key Mode, this pin is trigger pin to play Voice Groups one time or looping sequentially up to 1024 Voice Groups.
- In CPU Parallel Mode, this pin is used as address strobe to latch the Voice Group address input at S1 to S8 and starts the voice playback.
- In MP3 Mode, this pin is Play / Pause.

- **VDDP and VDDA :**

Power Supply Pins: These two pins must be connected together to the positive power supply.

- **VSS :**

Power Ground Pins: VSS and VPP pins must be connected to the power ground.

- **M0 and M1 :**

In Key Mode、CPU Parallel Mode、MP3 Mode、SPI Mode、and I2C Mode ,
M0 and M1 can be used for Crystal oscillator or volume control.

In aP89 Mode Operating Mode Setting Pins:
- M1=0, M0=0 set the chip into Key Trigger Mode
- M1=0, M0=1 set the chip into CPU Parallel Command Mode
- M1=1, M0=0 set the chip into CPU Serial Command Mode
- M1=1, M0=1 set the chip into OTP Programming Mode

- **VOUT1 and VOUT2 :**

14-bit PWM output pins which can drive speaker and buzzer directly for voice playback.

- **OSC :**

During voice playback, an external resistor is connected between this pin and the VDD pin to set the sampling frequency. Or keep OSC floating if choosing INT-Rosc.
Note : External resistor is 68K Ω

- **VPP :**

During voice playback, this pin must be connected together with VSS. In OTP Programming Mode, this pin is connected to a separate 8.5V power supply voltage for OTP programming.

- **OUT1, OUT2 and OUT3 :**

OUT1,OUT2 and OUT3 can select output function as below :
1. Busy- H : When voice is playing, output high level signal.
2. Busy- L : Inverted output of Busy- H.
3. LED- Flash : When voice is playing, output LED flash pulse.
4. ~LED- Flash : Inverted output of LED- Flash
5. Stop- H : When voice plays finished, output stop pulse.
6. Stop- L : Inverted output of Stop- H.
7. LoadBit : After load voice data to buffer success, output logic high signal.
8. Prog-Busy - H : When voice of Prog-Busy set 1, high pulse output.
   When voice of Prog-Busy set 0, low pulse output.
9. Prog-Busy - L : Inverted output of Prog-Busy - H.

- **COUT :**

16-bit current mode DAC output for voice playback

- **RST :**

Chip reset in playback mode.

▪ VOICE SECTION COMBINATIONS :

Voice files created by the PC base developing system are stored in the built-in EPROM of the aP89682K/341K/170K/085K chip as a number of fixed length Voice Blocks. Voice Blocks are then selected and grouped into Voice Groups for playback. Up to 1024 Voice Groups are allowed. A Voice Blocks Table is used to store the information of combinations of Voice Blocks and then group them together to form Voice Group.

Chip	aP89682K	aP89341K	aP89170K	aP89085K
Memory size	16M bits	8M bits	4M bits	2M bits
Max no. of Voice Block	2016	2016	2016	2016
Max. no. of Voice Group	1024	1024	1024	1024
Voice Length (@ 6KHz 4-bit ADPCM)	682 sec	341 sec	170 sec	85 sec

▪ Example of Voice Block Combination :

Assume here we have three voice files, they are “How are You?”, Sound Effect and Music. Each of the voice file is divided into a number of fixed length Voice Block and stored into the memory.
Voice block :

B1 = “How”	B2 = ”are”	B3 = ”You”
B4 = Sound Effect	B5 = Music1	B6 = Music2

Voice Blocks are grouped together using Voice Table to form Voice Group for playback:

Group no.	Voice Group contents	Voice Table Entries
Group 1	“How are You?”	B1+B2+B3
Group 2	Sound Effect + “How are You?”	B4+ B1+B2+B3
Group 3	“How are You?” + Music1	B1+B2+B3+B5
Group 4	Music2	B6

▪ Voice Data Compression :

Voice File data is stored in the on-chip EPROM as either 4-bit ADPCM or 8-bit PCM/ ULAW format or 16-bit PCM format. Voice data are stored as 16-bit PCM forma is without compression. The voice playback quality is best. Voice data stored as 4-bit ADPCM or 8-bit PCM/ ULAW provide 4:2 data compression to save memory space. But voice playback quality with be lower than 16-bit PCM format.

▪ Group Options :

User selectable options that affect each individual group are called Group Options. They are:

- Edge or Level trigger
- Unholdable or Holdable trigger
- Re-triggerable or Non-retriggerable
- Stop pulse disable or enable

Fig. 1 to Fig. 6 show the voice playback with different combination of triggering mode and the relationship between outputs and voice playback.

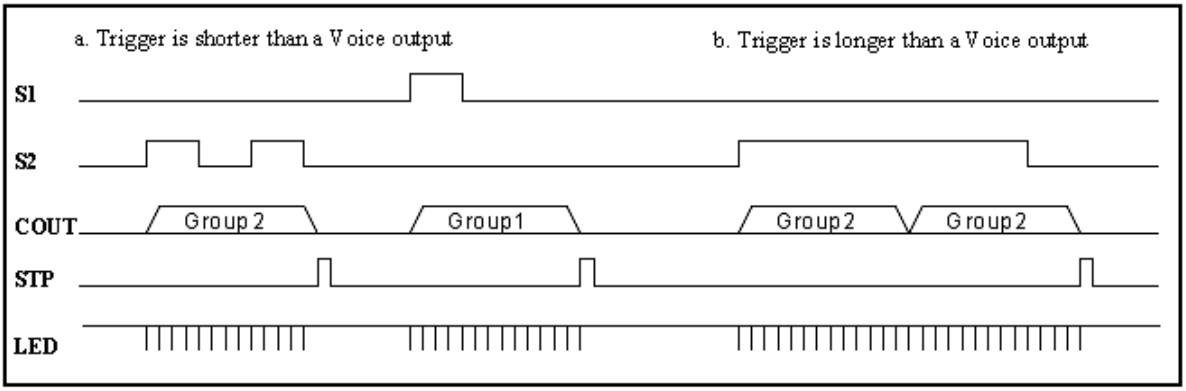


Fig. 1 Level, Unholdable, Non-retriggerable

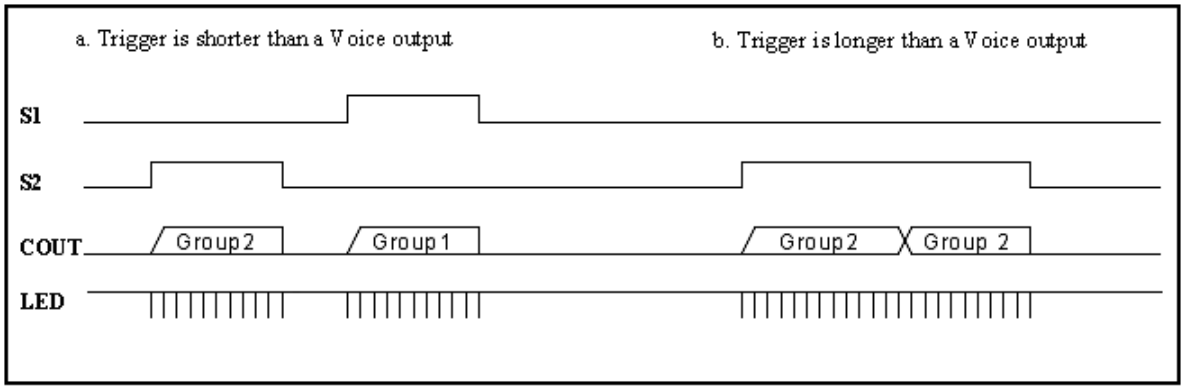


Fig. 2 Level Holdable

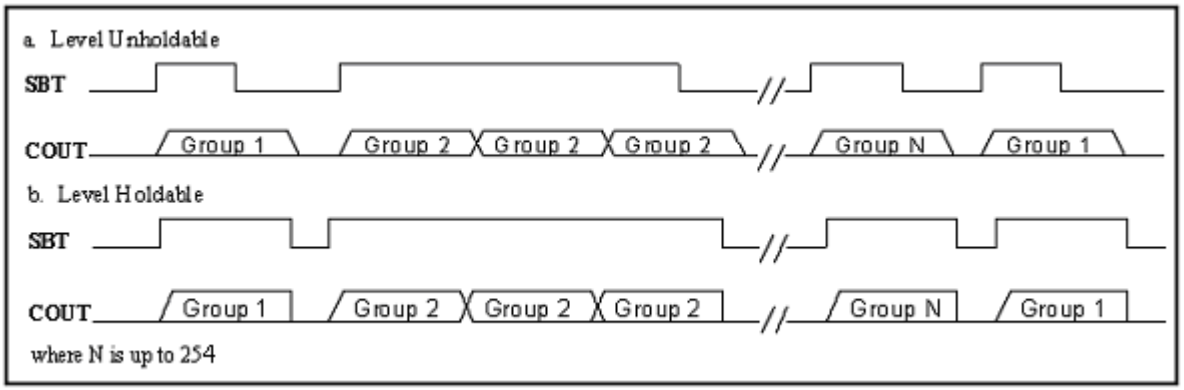


Fig. 3 SBT sequential trigger with Level Holdable and Unholdable

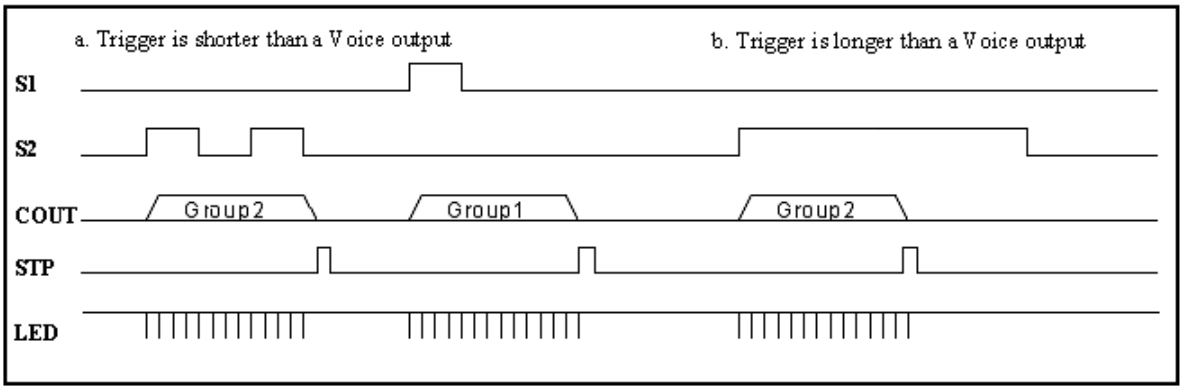


Fig. 4 Edge, Unholdable, Non-retrigger

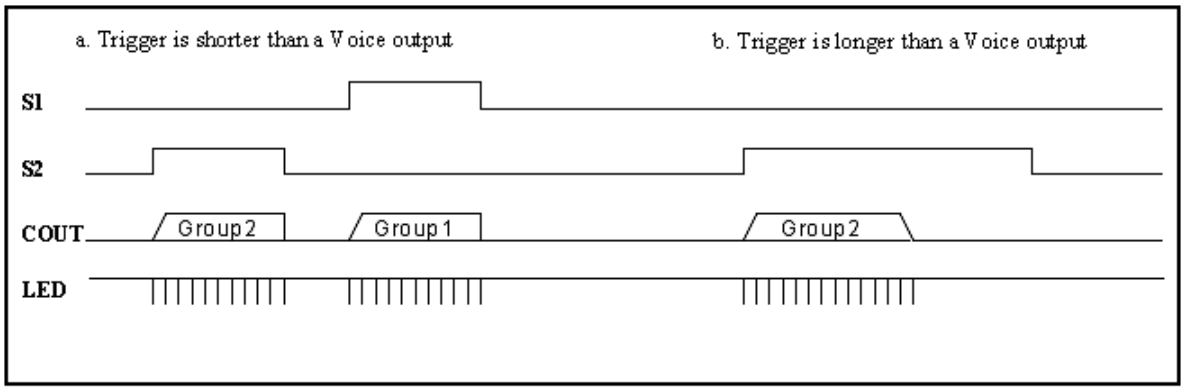


Fig. 5 Edge, Holdable

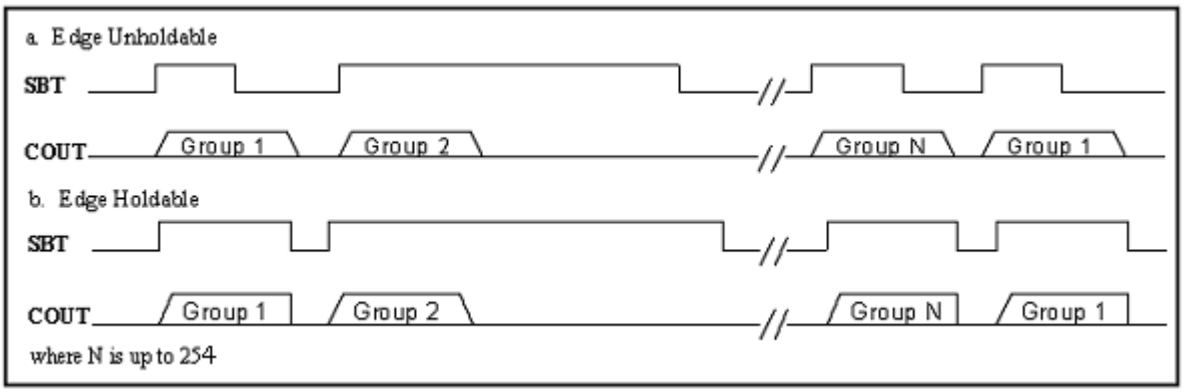


Fig. 6 SBT sequential trigger with Edge Holdable and Unholdable

▪ TRIGGER MODES :

There are six trigger modes available for aP89682K/341K/170K/085K series.

- Key Mode
- CPU Parallel Mode
- SPI Mode
- I2C Mode
- MP3 Mode
- aP89 Mode

Key Mode :

With this trigger mode, the beginning 57 Voice Groups are triggered by setting S1 to S8 to HIGH or LOW in different combinations. Each Voice Group can have its only independent trigger options (See Fig. 1,2,4 and 5 for trigger options definition).

A maximum of 1024 Voice Groups are available. And can be triggered one by one sequentially with the SBT key (See Fig. 3 and 6).

The setting of S1 to S8 for triggering the 1st to the 57nd Voice Groups are as follow:

Voice Group	S1	S2	S3	S4	S5	S6	S7	S8
SW1	HIGH	NC	NC	NC	NC	NC	NC	NC
SW2	NC	HIGH	NC	NC	NC	NC	NC	NC
SW3	NC	NC	HIGH	NC	NC	NC	NC	NC
SW4	NC	NC	NC	HIGH	NC	NC	NC	NC
SW5	NC	NC	NC	NC	HIGH	NC	NC	NC
SW6	NC	NC	NC	NC	NC	HIGH	NC	NC
SW7	NC	NC	NC	NC	NC	NC	HIGH	NC
SW8	NC	NC	NC	NC	NC	NC	NC	HIGH
SW9	HIGH	HIGH	NC	NC	NC	NC	NC	NC
SW10	NC	HIGH	HIGH	NC	NC	NC	NC	NC
SW11	NC	NC	HIGH	HIGH	NC	NC	NC	NC
SW12	NC	NC	NC	HIGH	HIGH	NC	NC	NC
SW13	NC	NC	NC	NC	HIGH	HIGH	NC	NC
SW14	NC	NC	NC	NC	NC	HIGH	HIGH	NC
SW15	NC	NC	NC	NC	NC	NC	HIGH	HIGH
SW16	HIGH	NC	NC	NC	NC	NC	NC	HIGH
SW17	HIGH	HIGH	HIGH	NC	NC	NC	NC	NC
SW18								
SW19	NC	NC	HIGH	HIGH	HIGH	NC	NC	NC
SW20	NC	NC	NC	HIGH	HIGH	HIGH	NC	NC
SW21	NC	NC	NC	NC	HIGH	HIGH	HIGH	NC
SW22	NC	NC	NC	NC	NC	HIGH	HIGH	HIGH
SW23	HIGH	NC	NC	NC	NC	NC	HIGH	HIGH
SW24	HIGH	HIGH	NC	NC	NC	NC	NC	HIGH
SW25	HIGH	HIGH	HIGH	HIGH	NC	NC	NC	NC
SW26	NC	HIGH	HIGH	HIGH	HIGH	NC	NC	NC
SW27	NC	NC	HIGH	HIGH	HIGH	HIGH	NC	NC
SW28	NC	NC	NC	HIGH	HIGH	HIGH	HIGH	NC
SW29	NC	NC	NC	NC	HIGH	HIGH	HIGH	HIGH
SW30	HIGH	NC	NC	NC	NC	HIGH	HIGH	HIGH
SW31	HIGH	HIGH	NC	NC	NC	NC	HIGH	HIGH
SW32	HIGH	HIGH	HIGH	NC	NC	NC	NC	HIGH
SW33	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC	NC
SW34	NC	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC
SW35	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH	NC
SW36	NC	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH
SW37	HIGH	NC	NC	NC	HIGH	HIGH	HIGH	HIGH
SW38	HIGH	HIGH	NC	NC	NC	HIGH	HIGH	HIGH
SW39	HIGH	HIGH	HIGH	NC	NC	NC	HIGH	HIGH
SW40	HIGH	HIGH	HIGH	HIGH	NC	NC	NC	HIGH
SW41	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC
SW42	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC
SW43	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
SW44	HIGH	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH
SW45	HIGH	HIGH	NC	NC	HIGH	HIGH	HIGH	HIGH
SW46	HIGH	HIGH	HIGH	NC	NC	HIGH	HIGH	HIGH
SW47	HIGH	HIGH	HIGH	HIGH	NC	NC	HIGH	HIGH
SW48	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC	HIGH
SW49	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC
SW50	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
SW51	HIGH	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
SW52	HIGH	HIGH	NC	HIGH	HIGH	HIGH	HIGH	HIGH

SW53	HIGH	HIGH	HIGH	NC	HIGH	HIGH	HIGH	HIGH
SW54	HIGH	HIGH	HIGH	HIGH	NC	HIGH	HIGH	HIGH
SW55	HIGH	HIGH	HIGH	HIGH	HIGH	NC	HIGH	HIGH
SW56	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC	HIGH
SW57	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH

★★★ Note: NC represents open or no connection

CPU Parallel Mode :

In this mode, S8 to S1 serve as 8-bit addresses input for 256 Voice Groups with S8 represents the MSB and S1 represents LSB. After Group address is set and ready, setting the SBT input pin LOW to HIGH will [LATCH] and trigger the corresponding Voice Group to playback.

Trigger options defined in Fig. 1,2, 4 and 5 are valid for this mode.

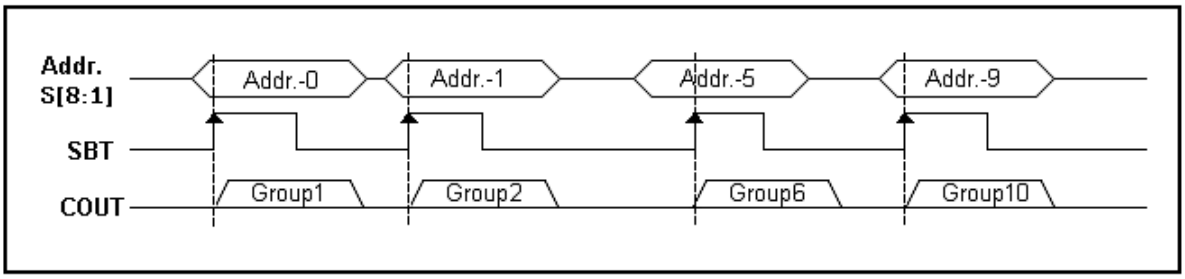


Fig. 7 CPU Parallel Trigger Mode

Note that SBT pin cannot be used as Single Button Sequential trigger in this mode. In stead, it acts as a Strobe input to clock-in the Voice Group address set at S8 to S1 into the chip.

Voice Groups are represented in Binary address format. For example:

[S8:S1] = 0000 0000 (00 hex) for Voice Group #1
[S8:S1] = 0000 0001 (01 hex) for Voice Group #2
• • •
[S8:S1] = 0000 1000 (08 hex) for Voice Group #9
• • •
[S8:S1] = 1000 1000 (88 hex) for Voice Group #137
• • •
[S8:S1] = 1111 1111 (FF hex) for Voice Group #256

aP89 Mode :

This trigger mode is function setting compatible with APLUS 1st Generation OTP IC (aP89341/aP89170/aP89085) usage only different control timing. Please refer to page 20 Fig.18.

SPI Mode :

This trigger mode is specially designed for simple CPU interface. The aP89682K/341K/170K/085K is controlled by command sent to it from the host CPU. S1 to S3 are used to input command word into the chip while OUT1 to OUT3 as output from the chip to the host CPU for feedback response.

- S1 acts as CS (Chip Select) to initiate the command word input
- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.
- OUT1 acts as BUSY to indicate the chip is in busy state.
- OUT2 acts as POUT to output user selected information.
- OUT3 acts as Loadbit signal to indicate the Voice Group address buffer is full.
- M0 acts as volume level increase.
- M1 acts as volume level decrease.

Command input into the chip 16-bit data. The first 8-bit data is command bits while the second 8-bit data (if any) is the Voice Group address data or set volume of value. Table 1 summarize the available commands and their functions.

Table1

cmd	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LOAD	1	0	0	1	0	1	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
PLAY	1	0	0	1	1	0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
PU1	1	0	1	0	0	1	Don’t care (ps : for VOUT without Ramp-up)									
PU2	1	0	1	0	1	0	Don’t care (ps : for COUT with Ramp-up)									
PD1	1	0	1	1	0	1	Don’t care (ps : for VOUT without Ramp-down)									
PD2	1	0	1	1	1	0	Don’t care (ps : for COUT with Ramp-down)									
VOL	0	1	0	0	0	1	0	0	0	0	0	0	vol4	vol3	vol2	vol1
VOL--	0	1	0	0	1	0	Don’t care									
VOL++	0	1	0	1	0	1	Don’t care									
PAUSE	0	1	1	0	0	1	Don’t care									
RESUME	0	1	1	0	1	0	Don’t care									
REWIND	0	1	1	1	0	1	Don’t care									

b : bit
X : Don’t care (maybe 1 or 0)

Load : for no gap loop playing ,the out pin (must be set up Loadbit)

Playing address-N….. check the out pin (Loadbit) is logic Low and can send next play group address-N+1,the Voice address-N is played and immediately playing the address-N+1

Play : The Play command load the Voice Group Address into the address buffer and play voice. (Address of value is section number - 1)

PU1 : Power up the chip with NO ramp-up (suitable for VOUT direct drive)

PU2 : Power up the chip WITH ramp-up (suitable for COUT transistor drive)

PD1 : Power down the chip with NO ramp-down (suitable for VOUT direct drive)

PD2 : Power down the chip WITH ramp-down (suitable for COUT transistor drive)

VOL : Set voice of volume (volume level : 0 ~ 15 ; max = 0 , min = 15).

VOL-- : Set volume level decrease.

VOL++ : Set volume level increase.

Pause : Set voice pause.

Resume : Set voice resume.

Rewind : The voice repeat.

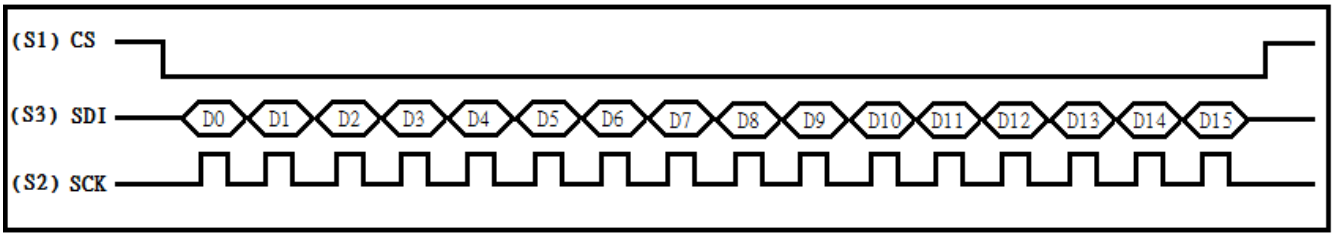


Fig. 8 SPI command timing

* The data bit only can be changed in SCK low level , but it has to be latched before rising edge of SCK.

(1). Load Voice Group Address

a. Command timing reference Fig. 8 SPI command timing.
b. D9 to D0 total 10 bits to be the Group Address
c. The OUT3 output (LoadBit) will become logic high once the Group Address is successfully loaded.
d. The Load signal will become logic LOW once the Voice Group is played and the address buffer is released and ready for next Play action.

(2). Play Voice Group Address

a. Command timing reference Fig. 8 SPI command timing.
b. D9 to D0 total10 bits as Group Address
c. Playing assign group address.

(3). Power up with RAMP-UP (PU2:A8xxh) or without RAMP-UP (PU1:A4xxh)

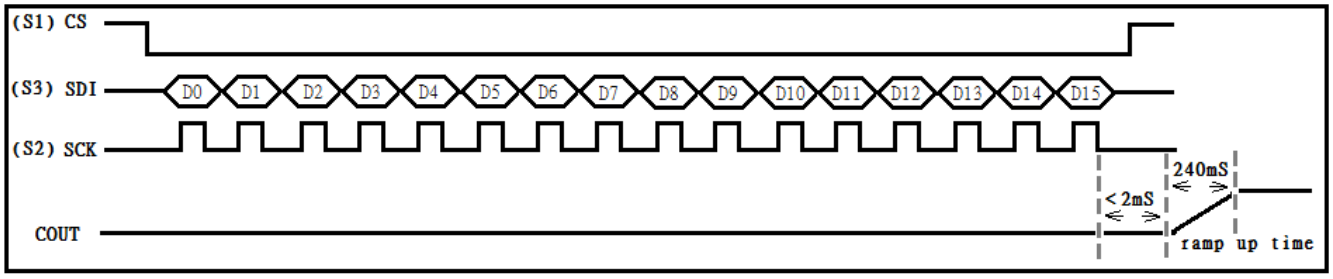


Fig. 9 Power-up command timing

PU1 : will power-up the chip and set the VOUT to 80H immediately and stay there.
PU2 : will power-up the chip and ramp-up COUT from 00H to 80H and stay there.

a. Voice will be playback immediately after PU1 / PU2 completes if the section buffer is filled with the Play command before power-up
b. OUT1 (BUSY-H) will output logic HIGH during playback voice operation.
c. PDN1 (Power-down without ramp-down) will be executed correctly only if PU1 is executed before.
d. PDN2 (Power-down with ramp-down) will be executed correctly only if PU2 is executed before.

(4). Power-down with RAMP-DOWN (PD2:B8xxh) or without RAMP-DOWN (PD1:B4xxh)

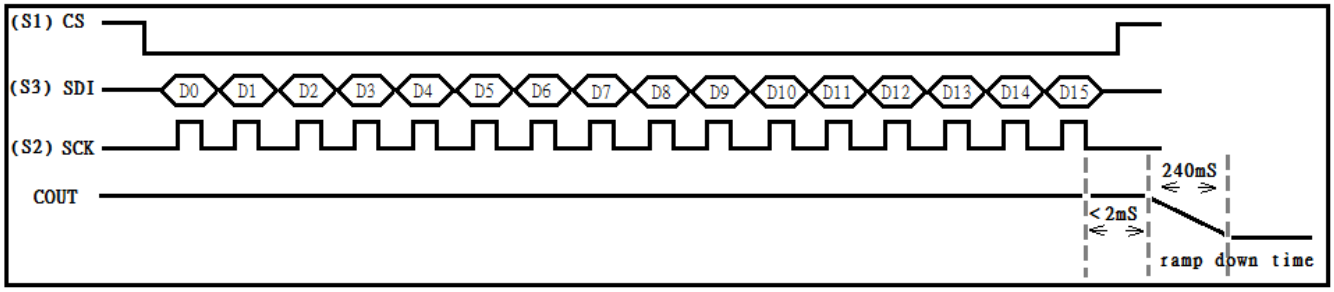


Fig. 10 Power-down commands timing

a. PDN1 will power-down the chip and set the VOUT data to 00H immediately.
PDN1 will be executed correctly only if PU1 is executed before.
b. PDN2 will power-down the chip and ramp-down the COUT from its current value to 00H.
PDN2 will be executed correctly only if PU2 is executed before.
c. The OUT1 pin (BUSY-H) will output logic HIGH during playback voice operation.

(5). Volume Set (VOL : 44xxh)

a. Command timing reference Fig. 8 SPI command timing.

b. D3 to D0 total 4bits (0 ~ 15) set volume level (max : 0 , min : 15)

(6). Volume - - (VOL - - : 48xxh)

a. Command timing reference Fig. 8 SPI command timing.

b. Set volume level decrease.

(7). Volume + + (VOL + + : 54xxh)

a. command timing reference Fig. 8 SPI command timing.

b. Set volume level increase.

(8). Pause and Resume (PAUSE:64xxh; RESUME:68xxh)

a. Command timing reference Fig. 8 SPI command timing.

b. In Pause state, VOUT1 and VOUT2 will stay at logic LOW while the COUT will stay at the current D/A data level (i.e. COUT is kept outputting an DC current). When Resume, the COUT data will continue at the current D/A data level.

c. The Pause state will be released by PDN1, PDN2 and RESUME commands.

(9). Rewind (REWIND : 78xxh)

a. Command timing reference Fig. 8 SPI command timing.

b. The voice repeat.

I2C Mode :

This trigger mode is specially designed for simple CPU interface. The aP89682K/341K/170K/085K is controlled by command sent to it from the host CPU. S2 and S3 are used to input command word into the chip while OUT1 to OUT3 as output from the chip to the host CPU for feedback response.

- The power on first send command PD2 or PD1 enter to I2C mode
- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.
- OUT1 acts as BUSY to indicate the chip is in busy state.
- OUT2 acts as POUT to output user selected information.
- OUT3 acts as Load signal to indicate the Voice Group address buffer is full.
- M0 acts as volume level increase.
- M1 acts as volume level decrease.

Command input into the chip 16-bit data. The first 8-bit data is command bits while the second 8-bit data (if any) is the Voice Group address data or set volume of value. Table 1 summarize the available commands and their functions.

1. Command reference Table 1
2. Command timing as below and reference Fig. 11 commands timing.

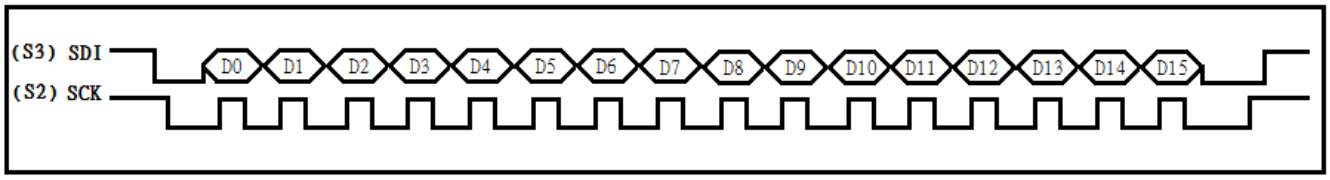


Fig. 11 commands timing

* The data bit only can be changed in SCK low level , but it has to be latched before rising edge of SCK

PU1 and PU2 command timing as below

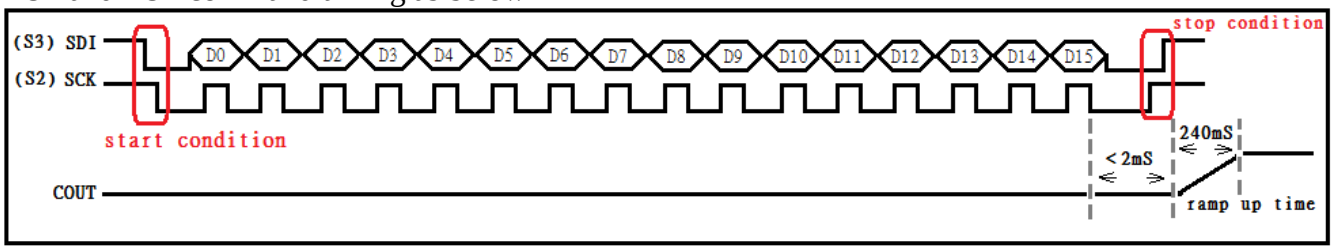


Fig. 12 Power-up commands timing

In Power up command : After start condition signal, add delay time more than 300us to wake up device.

PD1 and PD2 command timing as below

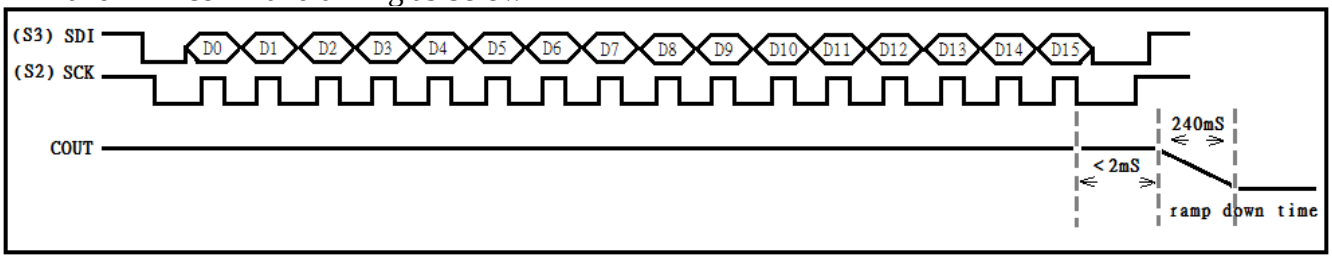


Fig. 13 Power-down commands timing

MP3 Mode :

This trigger mode is specially designed for simple MP3 function.

User can start to Play or Pause the voice by SBT pin, and Backward or Forward play by S1 pin or S2 pin, up to 1024 Voice Sections.

- SBT acts as play / pause
- S1 acts as backward.
- S2 act as forward.
- S3 acts as stop.
- S4 act as reset
- M0 acts as volume level increase.
- M1 acts as volume level decrease.

▪ Oscillator Resistance :

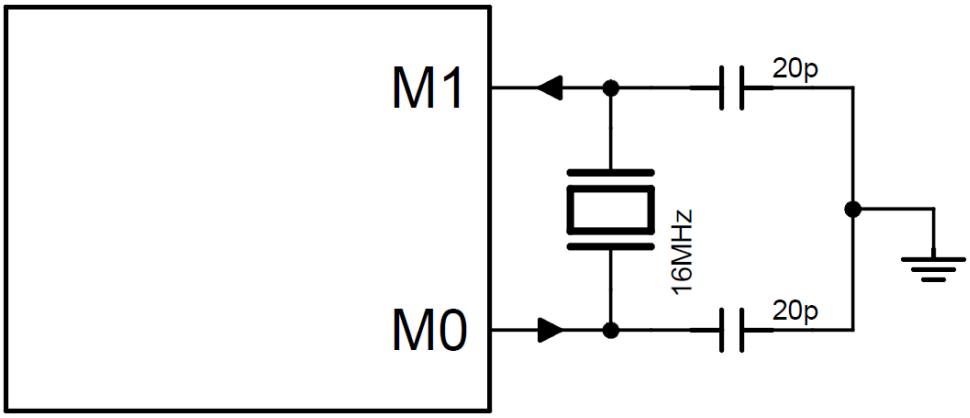
We have 3 modes can choose: Internal resistor、External resistor、Crystal resistance

Rosc Int – No need to add resistance

Rosc Ext – Use 68K ohm resistance in OSC pin

XT - Setting Crystal mode in M0 pin and M1 pin

1. Use 10pF ~ 30pF for capacitor.
2. The crystal use 16MHz.



▪ BLOCK DIAGRAM :

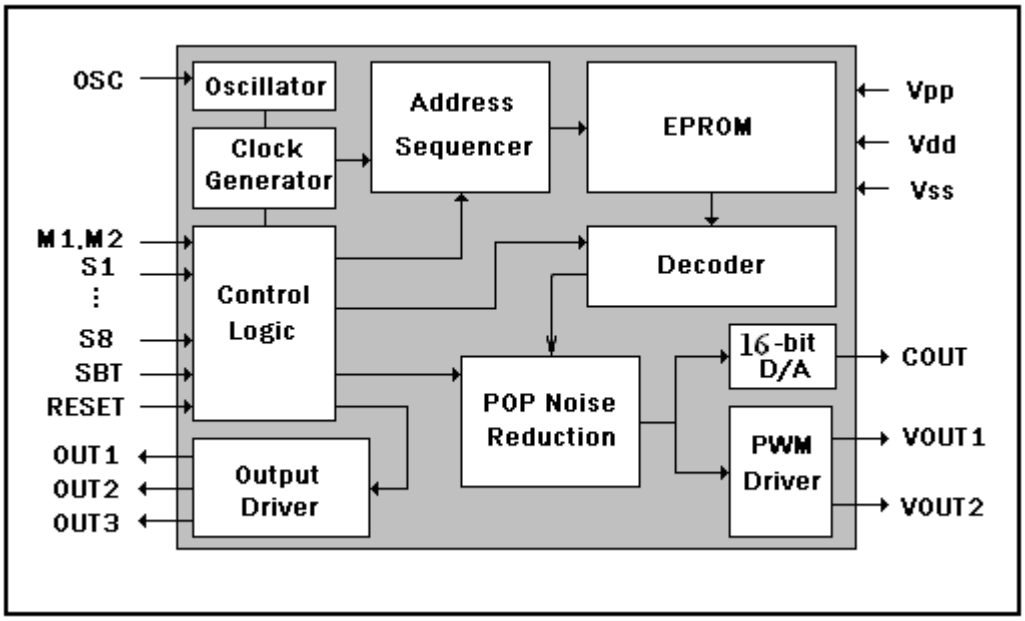


Fig. 14 Block Diagram

▪ ABSOLUTE MAXIMUM RATINGS :

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +5.0	V
V_{IN}	V_{SS} - 0.3 < V_{IN} < V_{DD} + 0.3	V
V_{OUT}	V_{SS} < V_{OUT} < V_{DD}	V
T (Operating):	-10 ~ +85	℃
T (Junction)	-10 ~ +85	℃
T (Storage)	-10 ~ +85	℃

DC CHARACTERISTICS (T_A = 0 to 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.0		5.0	V	
ΔFc/Fc	Chip to chip frequency variation	-1.5		+1.5	%	

Symbol	Parameter	VDD	Min.	Typ.	Max.	Unit	Condition
I_{SB}	Standby current	3.3			1.0	uA	
		4.5			1.0		
I_{OP}	Operating current	3.3		11		mA	
		4.5		18			
I_{IH}	Input current	3.3		7		uA	V_{IL}=3.3V
		4.5		17			V_{IL}=4.5V
V_{IH}	Input high voltage	3.3		2/3 VDD		V	
		4.5					
V_{IL}	Input low voltage	3.3		1/3 VDD		V	
		4.5					
I_{OH}	Output high current	3.3		-16		mA	V_{OH}=2.0V
		4.5		-25			V_{OH}=3.5V
I_{OL}	Output low current	3.3		26		mA	V_{OL}=1.0V
		4.5		36			
I_{VOUT}	VOUT Current	3.3		150		mA	Load=8Ω
		4.5		220			
I_{COUT}	COUT Current	3.3		4		mA	V_{COUT}=1.0V
		4.5		4			full scale
ΔF/F	Frequency Stability	3.3		1.5		%	Note1
		4.5		1.5			Note2

Note1:

$$\frac{Fosc(3.3) - Fosc(2.7)}{Fosc(3.3)}$$

Note2:

$$\frac{Fosc(5.0) - Fosc(4.5)}{Fosc(4.5)}$$

▪ TIMING WAVEFORMS :

- KEY Trigger Mode :

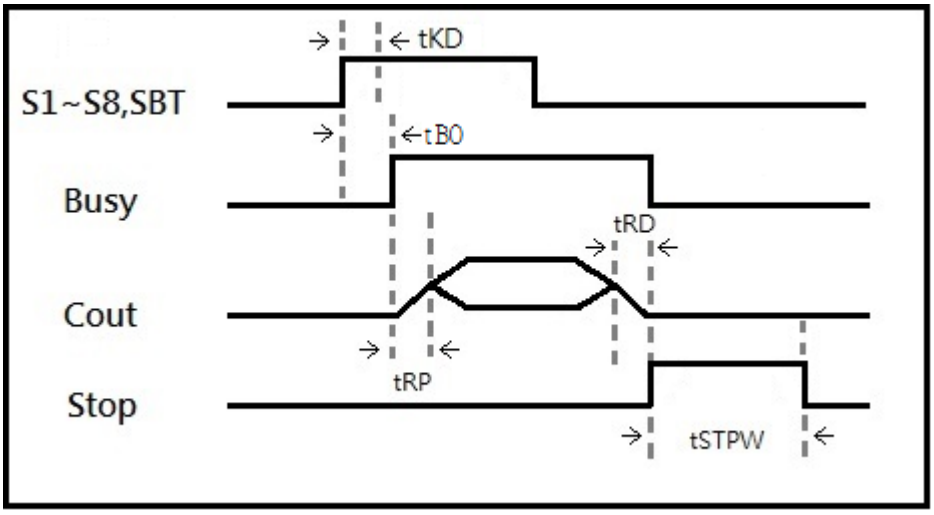


Fig. 15

- CPU Parallel Mode :

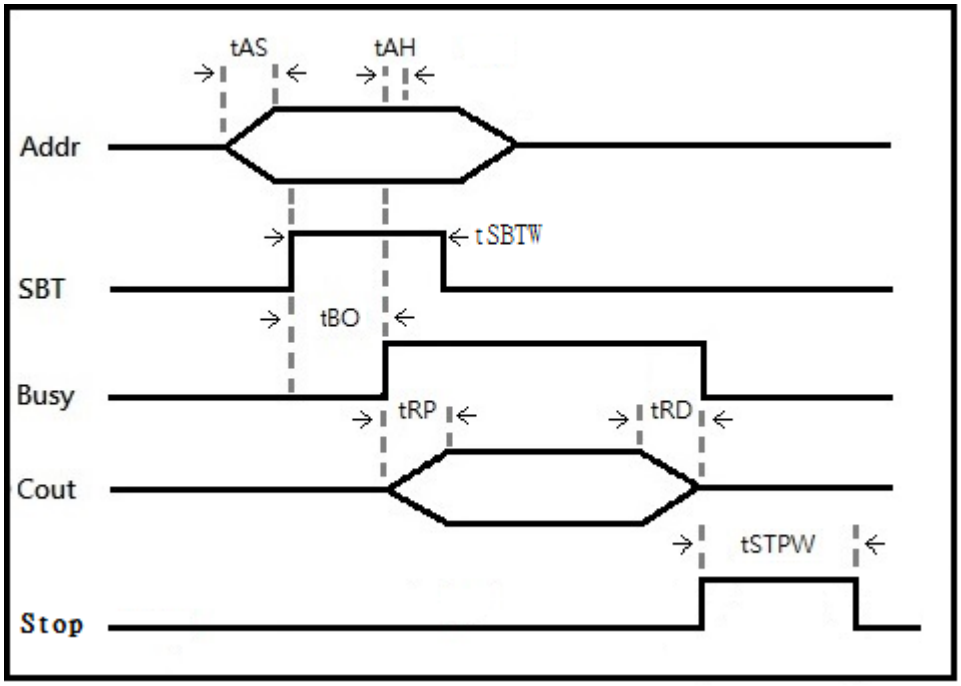


Fig. 16

- SPI Mode :

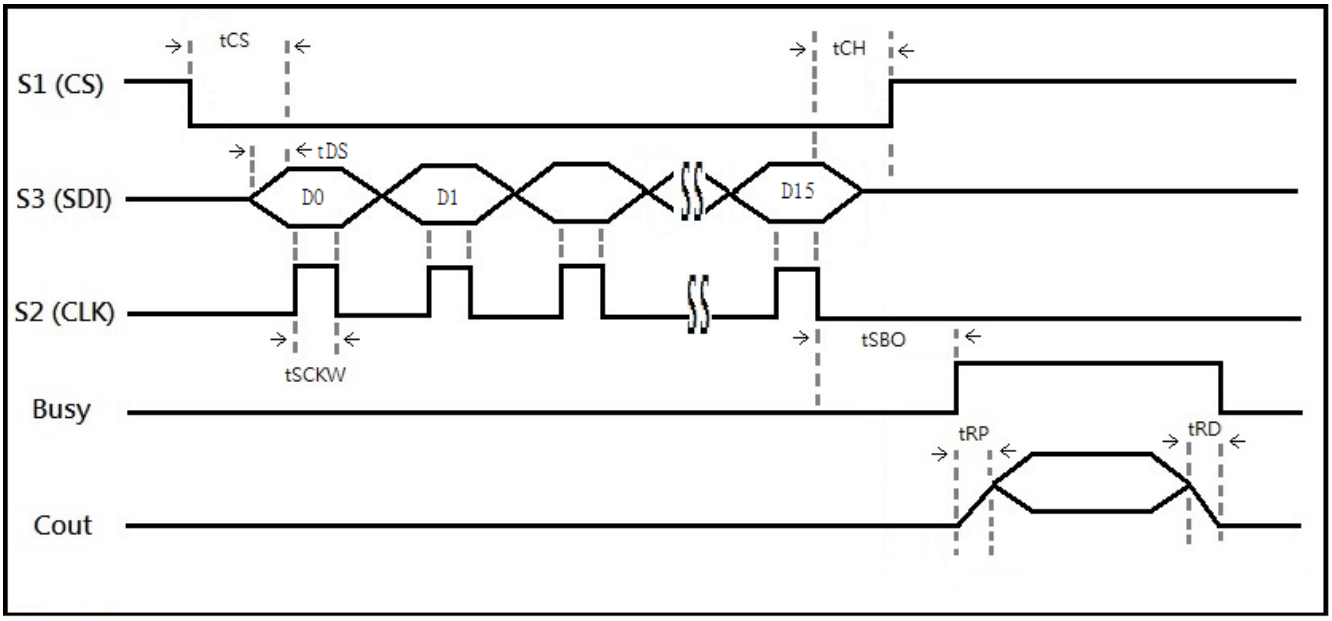


Fig. 17

- aP89 Mode CPU Serial :

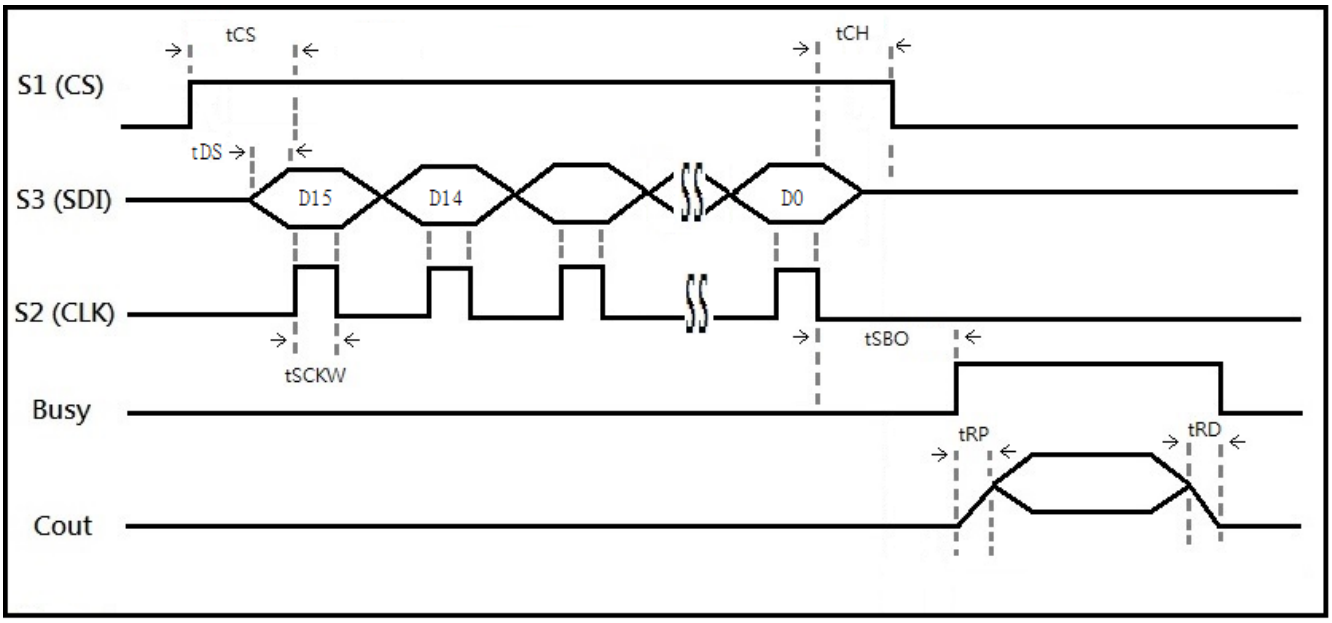


Fig. 18

- I2C Mode :

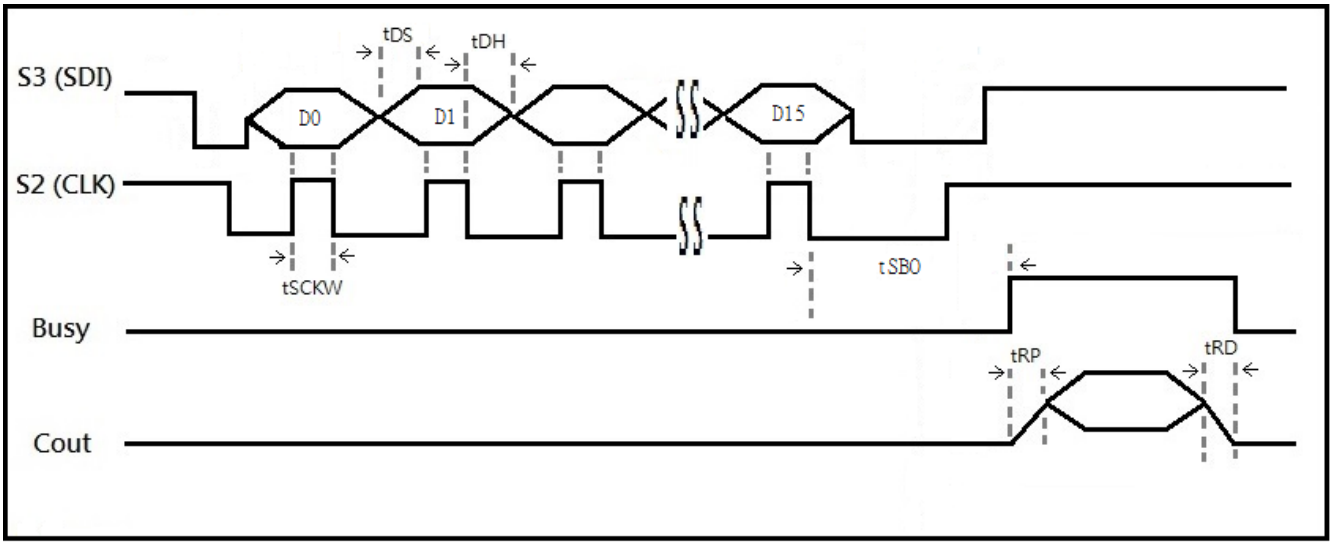


Fig. 19

▪ AC CHARACTERISTICS (T_A = 0 to 70℃, V_{DD} = 3.3V, V_{SS} = 0V, 8KHz sampling)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
t_{KD}	Key trigger debounce time (long)	16	—	—	ms	1
t_{KD}	Key trigger debounce time (short)	1	—	—	ms	1
t_{STPW}	STOP pulse width (long)	—	128	—	ms	1
t_{STPW}	STOP pulse width (short)	—	500	—	μs	1
t_{AS}	Address set-up time	300	—	—	ns	
t_{AH}	Address hold time	300	—	—	ns	
t_{SBTW}	SBT stroke pulse width (long)	16	—	—	ms	1
t_{SBTW}	SBT stroke pulse width (short)	1	—	—	ms	1
t_{BO}	BUSY signal output delay time(long)	—	24	—	ms	1
t_{BO}	BUSY signal output delay time(short)	—	1	—	ms	1
t_{CS}	Chip select set-up time	100	—	—	ns	
t_{CH}	Chip select hold time	100	—	—	ns	
t_{SCKW}	Serial clock pulse width	1	—	—	μs	
t_{DS}	Data set-up time	100	—	—	ns	
t_{DH}	Data hold time	100	—	—	ns	
t_{SBO}	BUSY signal output delay time	—	—	2	ms	
t_{RP}	Ramp Up time	—	240	—	ms	
t_{RD}	Ramp Down time	—	240	—	ms	
t_{FD}	Full signal output delay time	—	—	2	ms	

Notes :

1. The long or short debounce time is selectable as whole chip option during Voice Files Compiling.

▪ TYPICAL APPLICATIONS :

Key Mode

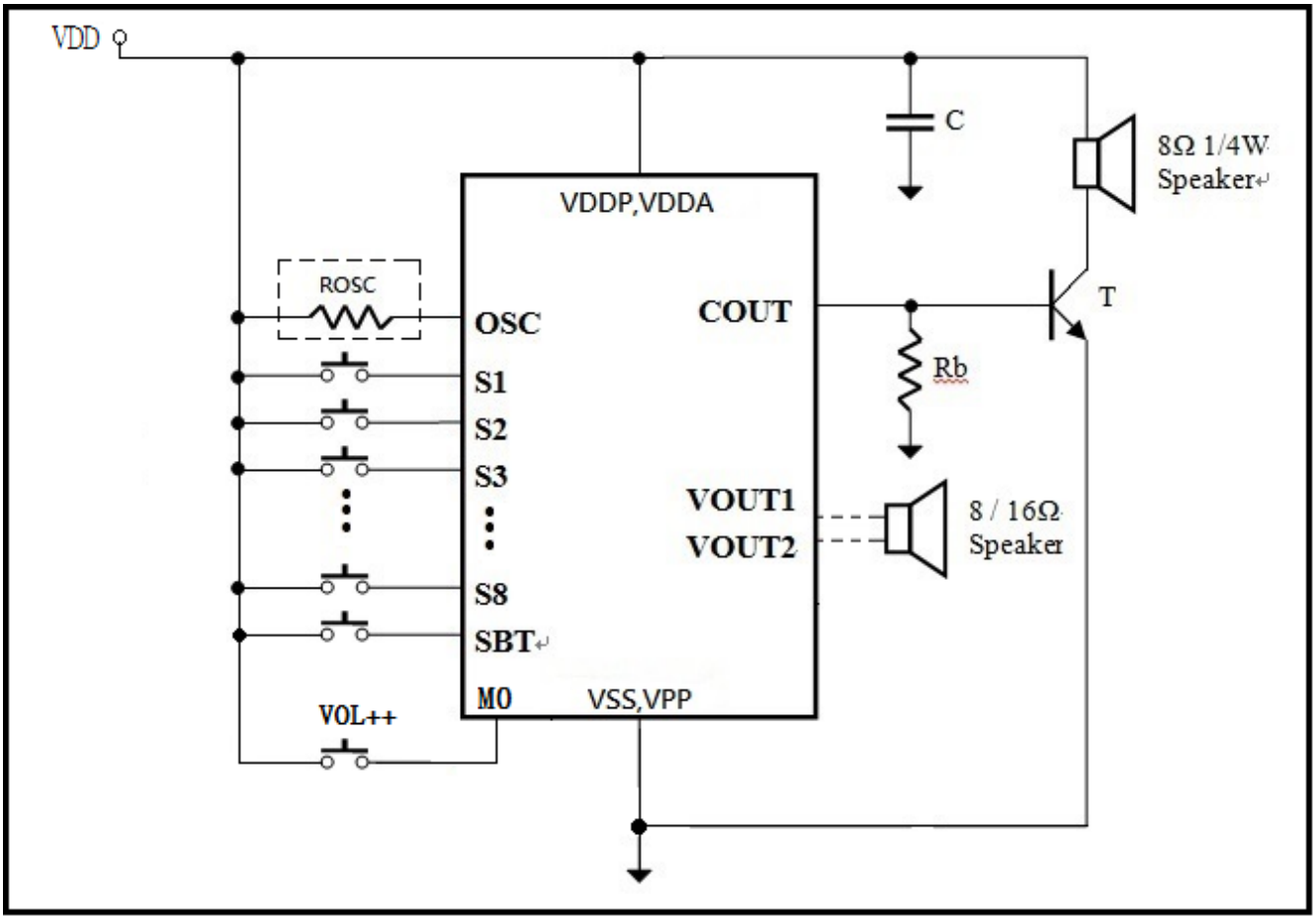


Fig. 20

Ex: Single key control volume.

If volume level is 8 , 1→2→3→4→5→6→7→8→1→2→3→ 4→….

CPU Parallel Mode

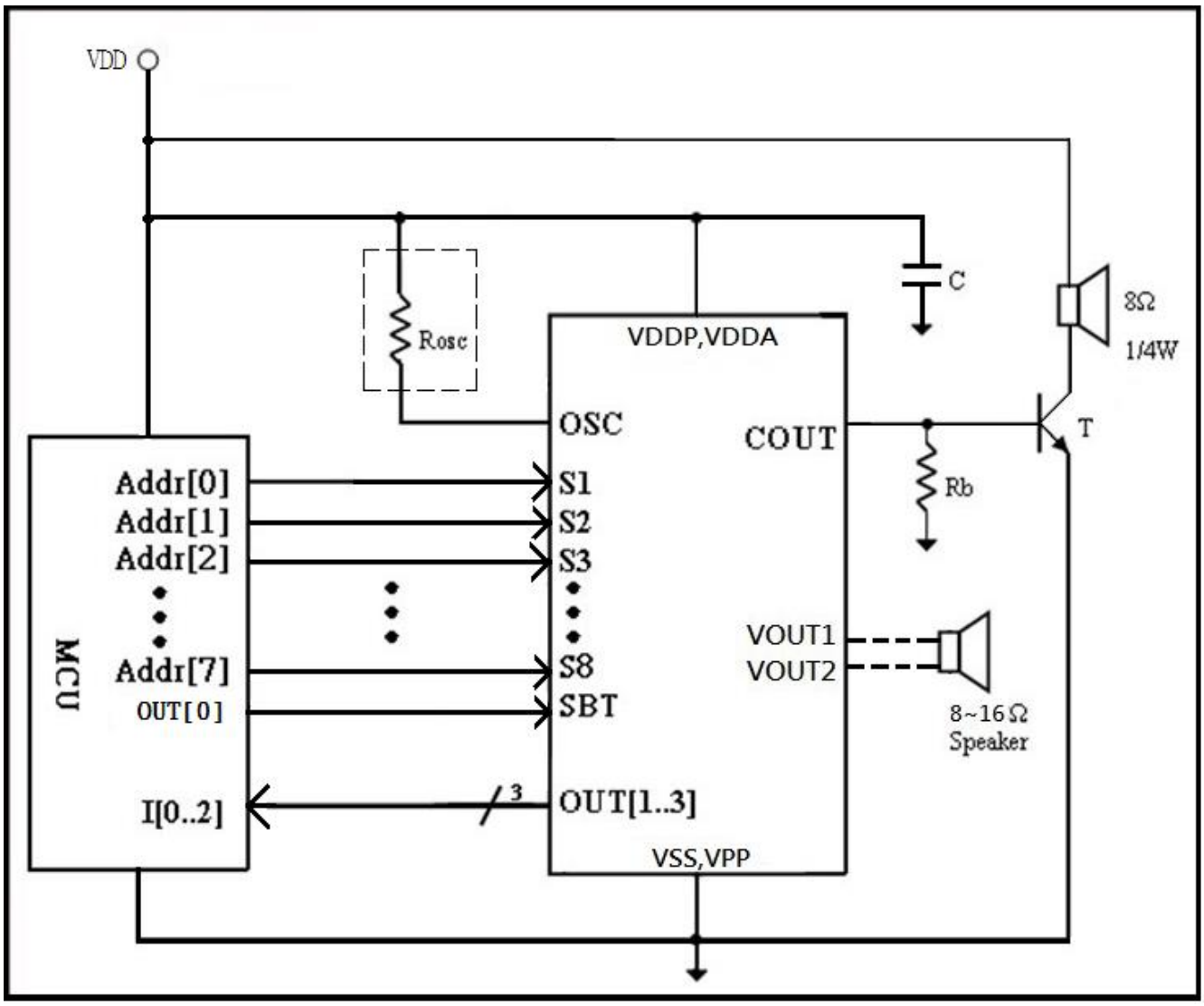


Fig. 21

Note:

1. C is capacitor from 0.1uF to 4.7uF depends on the kind of Vdd source and sound loudness.
2. Rb is base resistor from 120 Ohm to 390 Ohm depends on Vdd value and transistor gain.
3. T is an NPN transistor with beta larger than 150.
4. Reference value for the above components are Rb = 390 Ohm and T = 8050D.

SPI Mode

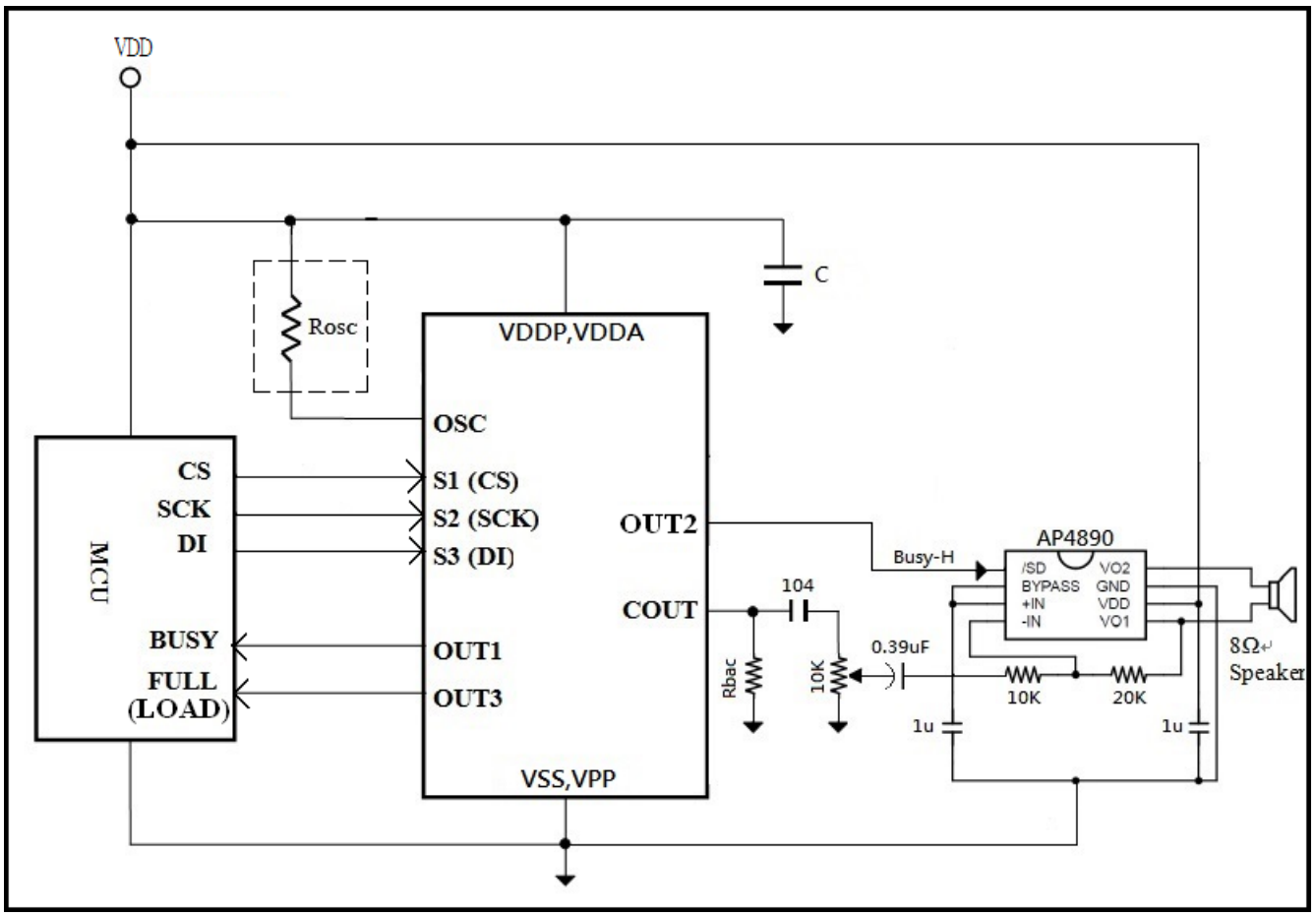


Fig. 22

I2C Mode

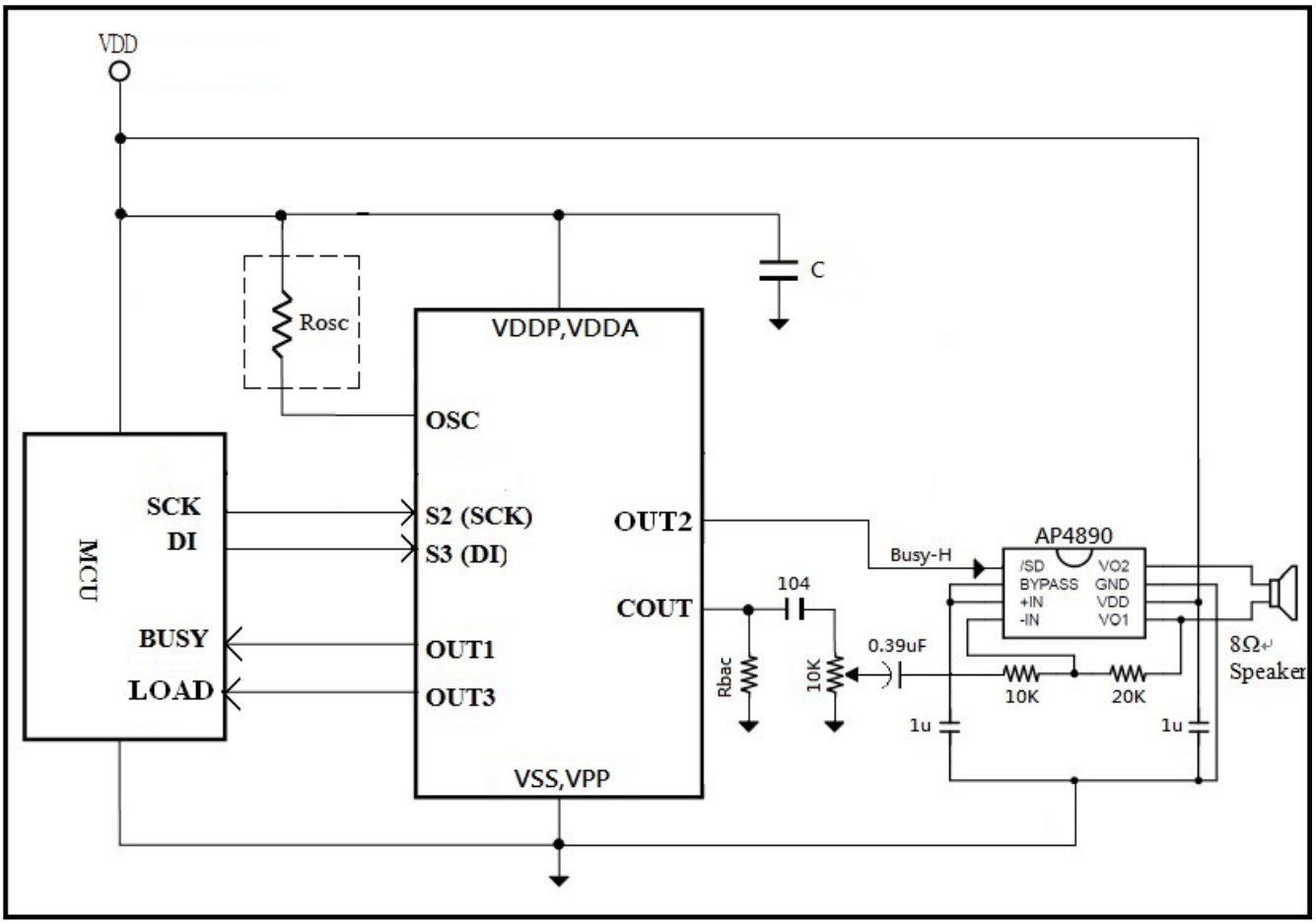


Fig. 23

MP3 Mode

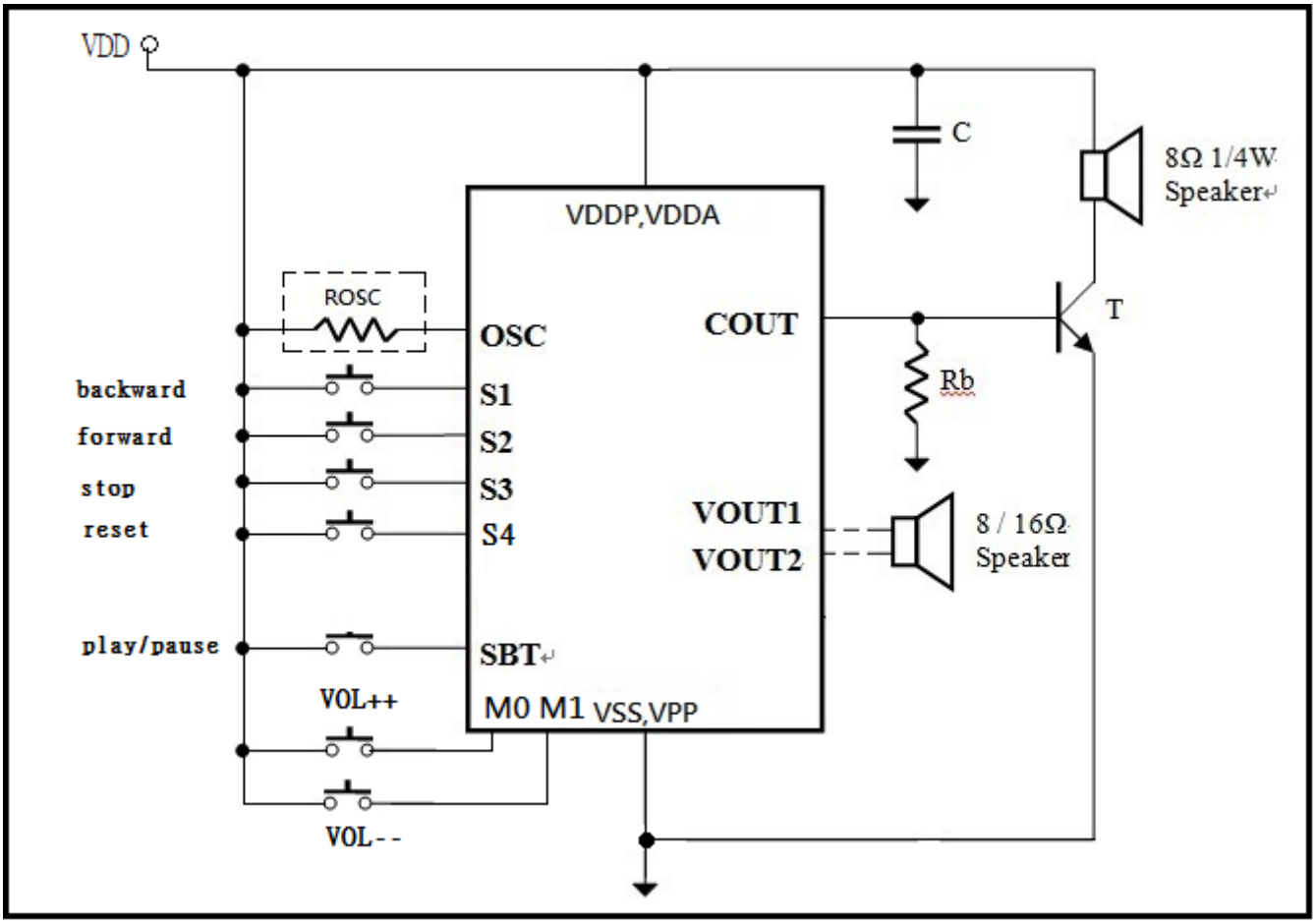
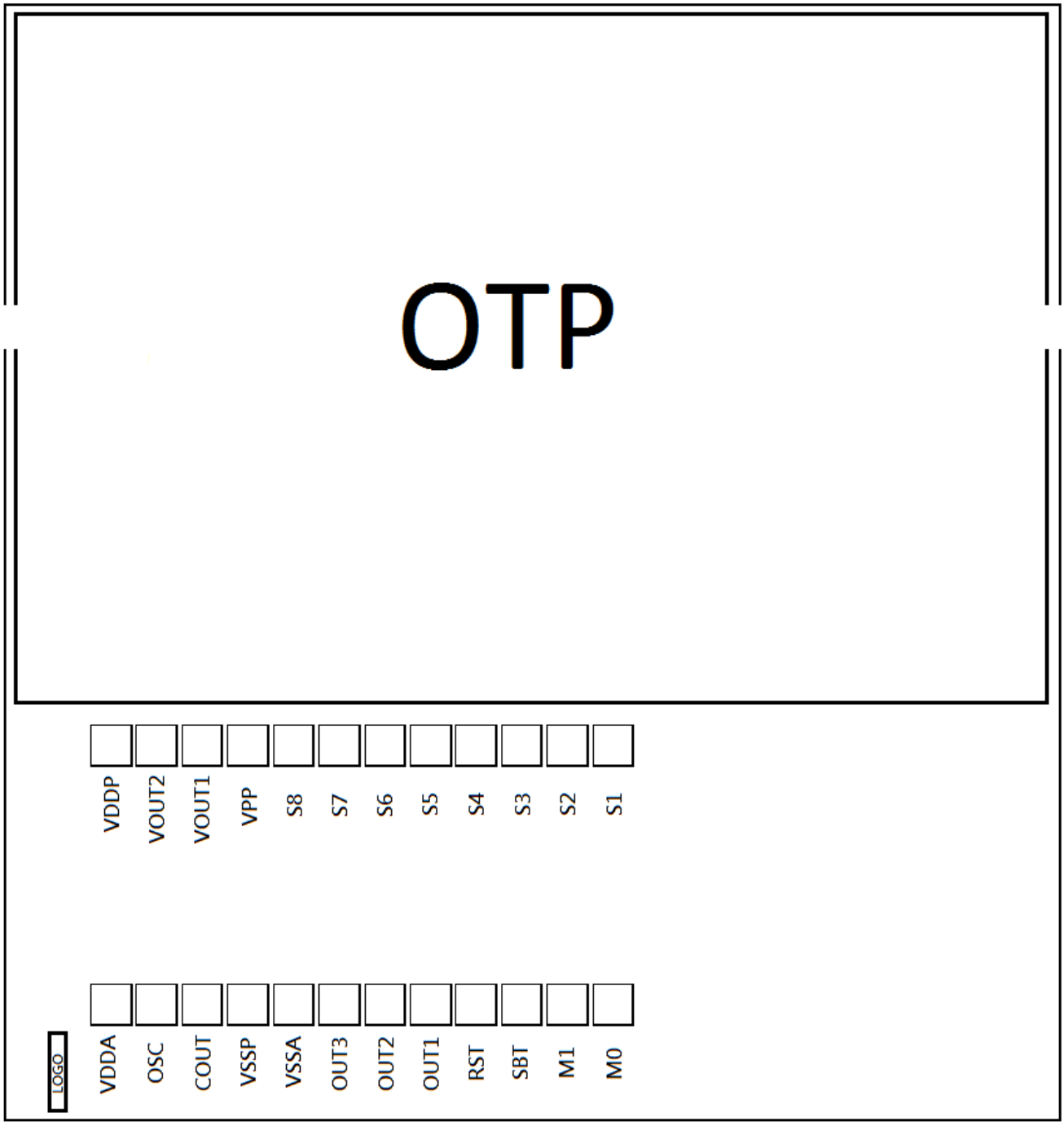


Fig. 24

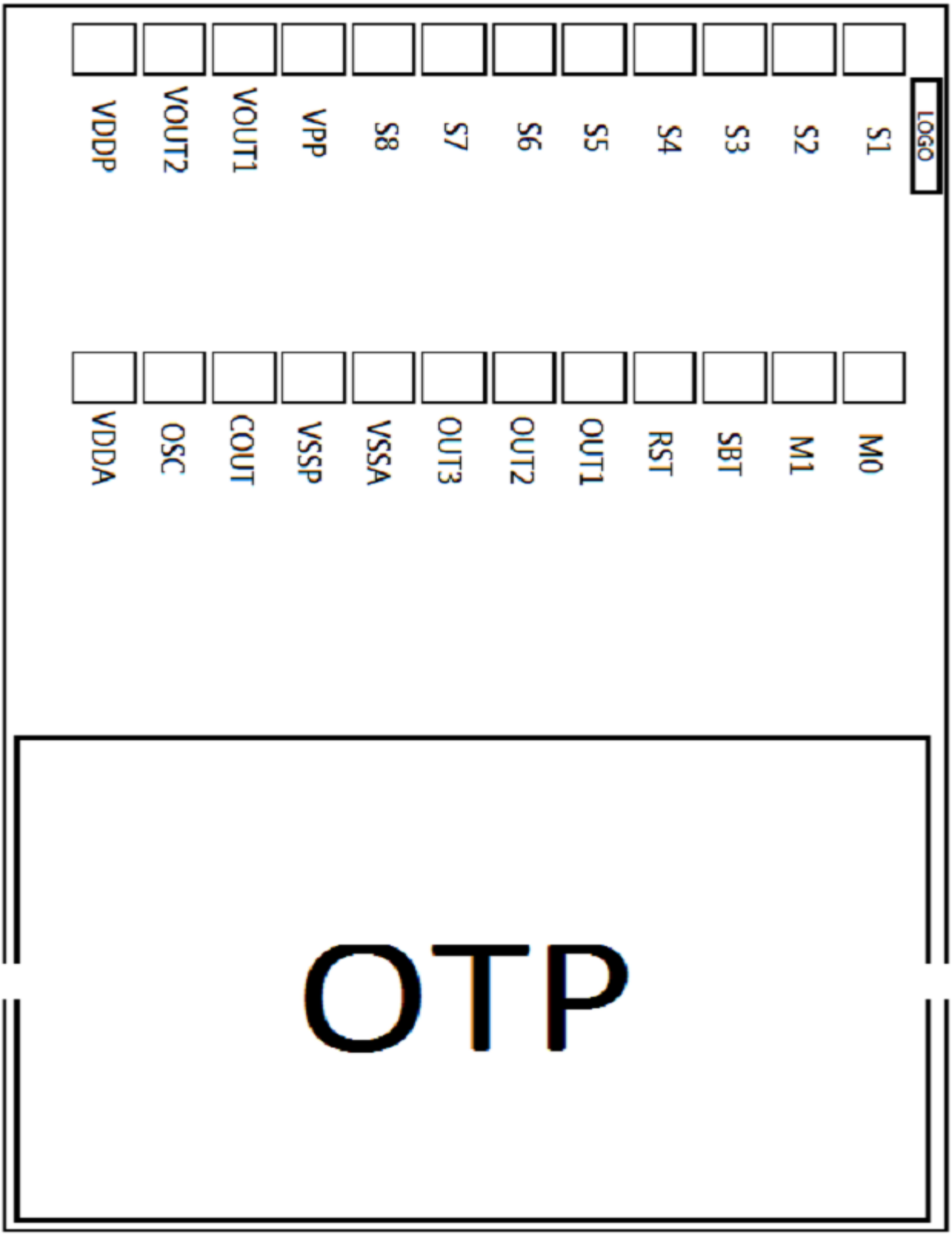
BONDING PAD DIAGRAMS (aP89682K/aP89341K)



Notes:

1. Between VPP and GND should add 10KΩ.
2. VDDA and VDDP should be connected to the Positive Power Supply.
3. VSSA and VSSP should be connected to the Power GND.
4. Substrate should be connected to the Power GND.

BONDING PAD DIAGRAMS (aP89170K/aP89085K)

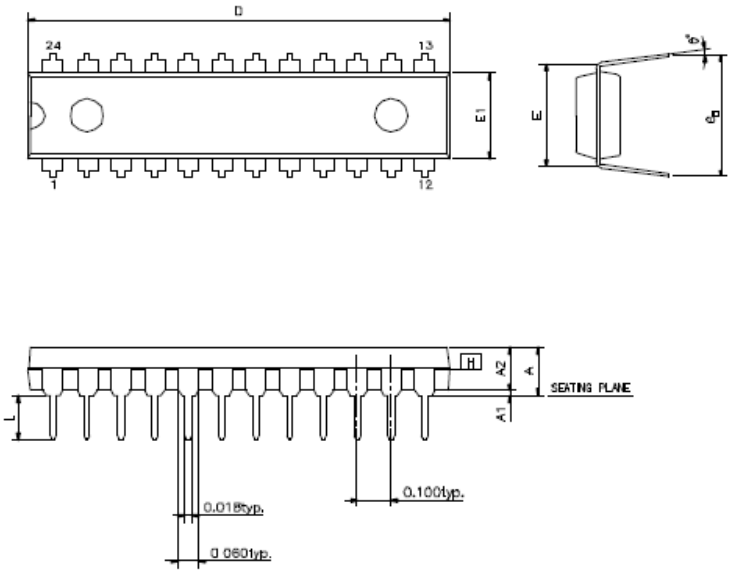


Notes:

1.Between VPP and GND should add 10KΩ.
2.VDDA and VDDP should be connected to the Positive Power Supply.
3.VSSA and VSSP should be connected to the Power GND.
4.Substrate should be connected to the Power GND.

PACKAGES DIMENSION OUTLINES

24-Pin 300mil P-DIP Package

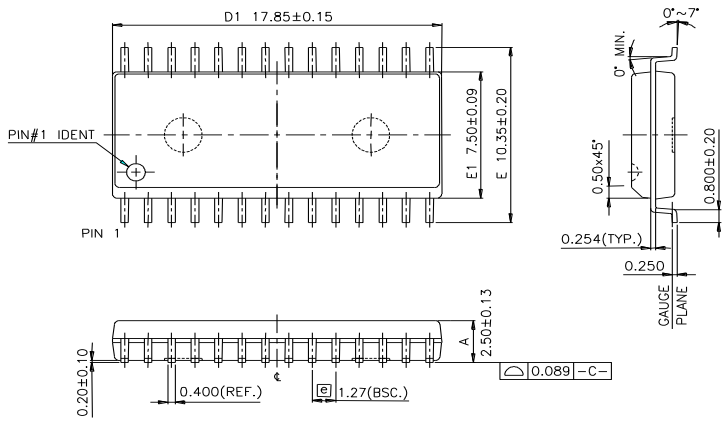


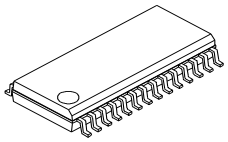
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	1.230	1.250	1.280
E		0.300 BSC.	
E1	0.253	0.258	0.263
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS–001 AF
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE H COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

28-Pin 300mil SOP Package





NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLMETERS (MM).
2. DIMENSION D1 & E1 DOES NOT INCLUDE MOLD PROTRUSION.
3. COPLANARITY OF ALL LEADS SHALL BE (BEFORE TEST) 0.089 MAX. FORM THE SEATING PLANE. UNLESS OTHERWISE SPECIFIED.
4. GENERAL PHYSICAL OUTLINE SPEC IS REFER TO TMC'S FINAL INSPECTION SPEC UNLESS OTHERWISE SPECIFIED.

HISTORY

2015/03/10
aP89682K_341K__170K_085K SPEC.

2015/07/20
aP89682K_341K__170K_085K SPEC : Modify cpu control timing waveforms
Modify Page. 18 DC CHARACTERISTICS
Reduce output function from 14 to 9.
Remove aP89 mode1 and aP89 mode2 and new adding aP89mode